In regard to FIG. **6** there is shown the interconnection of wafers wherein micro-post **16'** is used to interconnect a wireless wafer **50** to a CMOS wafer **52**. Each of the wafers are processed separately and are bonded using the bonding method described hereinabove.

FIG. **7** illustrates the interconnection of two wafers wherein micro-post **16'** is used to connect a micro-electro-mechanical sensor (MEMS) wafer **60** to a CMOS wafer **62**. MEMS wafer **60** includes a semiconductor material **62**, e.g. Si, a diaphragm region **64** embedded in said semiconductor material **62** and sensor elements **66** on surface of insulating layer, e.g. SiO_2, **68**. The CMOS wafer includes a control circuitry region **70**.

While the invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made without departing from the scope and spirit of the present invention. It is therefore intended that the invention not be limited to the exact forms described and illustrated, but should fall within the scope of the appended claims.

Having thus described our invention, what we claim as new, and desire to secure the Letters Patent is:

1. A method of manufacturing a microelectronic device comprising the steps of:

(a) etching at least one hole defined by a wall and a channel at least partly through a wafer of a semiconductor material;

(b) forming a layer of electrically insulating material to cover said wall; and

(c) forming an electrically conductive material on said covered wall within said channel of said hole.

2. The method of claim **1** wherein said etching includes dry or wet etching.

3. The method of claim **2** wherein said etching is a dry etch selected from the group consisting of reactive ion etching, chemical dry etching and ion beam etching.

4. The method of claim **3** wherein said drying etching includes a gas selected from the group consisting of CF_4, SF_6, NF_3, CHF_3, C_4F_8, $CHCl_3$, O_2, Cl_2, Br_2 and mixtures thereof.

5. The method of claim **2** wherein said etching is a wet etch comprising a chemical etchant selected from the group consisting of HF, NaOH, KOH, H_2O_2, ethylene diamine and ethanolamine.

6. The method of claim **5** wherein said wet etch is carried out by anodic etching.

7. The method of claim **1** wherein said etching further provides optional lateral spaces adjacent to said holes.

8. The method of claim **1** wherein said electrically insulating material is selected from the group consisting of diamond-like carbon, SiO_2, Si_3N_4 and Al_2O_3.

9. The method of claim **8** wherein said electrically insulating material is SiO_2.

10. The method of claim **1** wherein said electrically insulating material is formed by oxidation.

11. The method of claim **10** wherein said oxidation comprises through high temperature oxidation or through deposition and etching.

12. The method of claim **1** wherein said electrically conductive material is selected from the group consisting of W, Cr, Cu, Al, Ni, In, Au and mixtures or alloys thereof.

13. The method of claim **1** wherein said electrically conductive material is formed by electroplating or electroless plating.

14. The method of claim **1** further comprising planarizing the structure formed after step (c).

15. The method of claim **14** wherein said planarizing includes chemical-mechanical polishing.

16. The method of claim **1** wherein said holes are etched partly through said wafer and comprising the further step of grinding a surface of said wafer to cause said hole to pass entirely through said wafer.

17. The method of claim **1** comprising a further step of stacking at least two wafers with at least one corresponding hole in alignment.

18. The method of claim **17** further comprising the step of heating said wafers in the presence of indium or a eutectic alloy under conditions effective to form an electrical connection between the conducting material of corresponding holes or to form contacts in a circuit.

19. The method of claim **17** further comprising the step of dicing said wafers into individual chip elements.

20. The method of claim **1** wherein said semiconductor wafer has circuitry on at least one of its surfaces.

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